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L5	10341	L4 AND (SOFTWARE\$1 APPLICATION\$1 PROGRAM\$3)	USPAT; IBM_TDB	OR	OFF	2005/09/26 12:56
L6	2927	L5 AND (PIN ((PERSON\$3 IDENTIFIER\$1 ID IDENTITY IDENTIFICATION\$1 SERIAL\$1) NEAR2 (CODE\$1 NUMBER\$1)))	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:19
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L13	338	L11 AND L12	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:03
L14	1205	(ACTIVAT\$4 START\$3) NEAR2 (SOME\$1 PART\$1 SECTION\$1 MODULE\$1) NEAR3 (SOFTWARE\$1 APPLICATION\$1 PROGRAM\$3)	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:04
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L16	59	L13 AND L15	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:16
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L19	115	L18 AND (PROFIL\$3 COUNTER\$1 (PREDETERMIN\$3 NEAR2 (THRESHOLD\$1 TIME\$1 ATTEMPT\$3)))	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:17
L20	23226	(INSTALL\$6) NEAR3 (SOFTWARE\$1 APPLICATION\$1 PROGRAM\$3 VIDEO\$1 MUSIC\$1 MPEG\$1)	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:17
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L23	160751	(USER\$2 PERSON\$3 CLIENT\$2) NEAR3 (DATA NUMBER CODE INFORMATION\$1 ADDRESS\$2)	USPAT; IBM_TDB	OR	OFF	2005/09/26 13:22
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Matthias Hauswirth, Peter F. Sweeney, Amer Diwan, Michael Hind

 October 2004 **ACM SIGPLAN Notices , Proceedings of the 19th annual ACM SIGPLAN Conference on Object-oriented programming, systems, languages, and applications**, Volume 39 Issue 10

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Object-oriented programming languages provide a rich set of features that provide significant software engineering benefits. The increased productivity provided by these features comes at a justifiable cost in a more sophisticated runtime system whose responsibility is to implement these features efficiently. However, the virtualization introduced by this sophistication provides a significant challenge to understanding complete system performance, not found in traditionally compiled languages ...

Keywords: hardware performance monitors, perturbation, software performance monitors, vertical profiling, whole-system analysis

2 [Reconfigurable computing: architectures and applications: Using reconfigurability to achieve real-time profiling for hardware/software codesign](#)

Lesley Shannon, Paul Chow

 February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

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Embedded systems combine a processor with dedicated logic to meet design specifications at a reasonable cost. The attempt to amalgamate two distinct design environments introduces many problems, one being how to partition a single design for the two platforms to achieve the best performance with the least effort. Since the latest FPGA technology allows the integration of soft or hard CPU cores with dedicated logic on a single chip, this presents new opportunities for addressing hardware/software ...

Keywords: FPGA, embedded processor, hardware/software codesign, performance measurement, profiling, soft processor

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